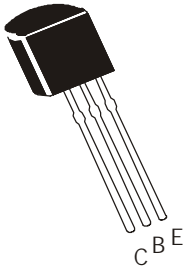


NPN SILICON PLANAR EPITAXIAL TRANSISTORS

BC546, A, B, C
BC547, A, B, C
BC548, A, B, C



TO-92
Plastic Package
 For Lead Free Parts, Device Part # will be Prefixed with "T"

Amplifier Transistors

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

DESCRIPTION	SYMBOL	BC546	BC547	BC548	UNITS
Collector Emitter Voltage	V _{CEO}	65	45	30	V
Collector Emitter Voltage	V _{CES}	80	50	30	V
Collector Base Voltage	V _{CBO}	80	50	30	V
Emitter Base Voltage	V _{EBO}	6	6	5	V
Collector Current Continuous	I _C	100			mA
Collector Current Peak	I _{CM}	200			mA
Base Current Peak	I _{BM}	200			mA
Emitter Current Peak	I _{EM}	200			mA
Power Dissipation at T _a =25°C	P _D	500			mW
Derate Above 25°C		4.0			mW/°C
Storage Temperature	T _{stg}	- 65 to +150			°C
Junction Temperature	T _j	150			°C

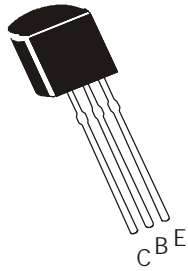
THERMAL RESISTANCE

Junction to Ambient in free air	R _{th(j-a)}	250	°C/W
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ELECTRICAL CHARACTERISTICS (T_a=25°C unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	BC546	BC547	BC548	UNITS
Collector Emitter Voltage	V _{CEO}	I _C =1mA, I _B =0	>65	>45	>30	V
Collector Base Voltage	V _{CBO}	I _C =10μA, I _E =0	>80	>50	>30	V
Emitter Base Voltage	V _{EBO}	I _E =10μA, I _C =0	>6.0	>6.0	>5.0	V
Collector Cut Off Current	I _{CBO}	V _{CB} =30V, I _E =0 ALL V _{CB} =30V, I _E =0, T _j =150°C ALL	<50 <5.0			nA μA
Collector Cut Off Current	I _{CES}	V _{CE} =80V, V _{BE} =0 V _{CE} =50V, V _{BE} =0 V _{CE} =30V, V _{BE} =0 V _{CE} =80V, V _{BE} =0, T _j =125°C V _{CE} =50V, V _{BE} =0, T _j =125°C V _{CE} =30V, V _{BE} =0, T _j =125°C	<15 <4.0	<15 <4.0	<15 <4.0	nA nA nA μA μA μA

NPN SILICON PLANAR EPITAXIAL TRANSISTORS



BC546, A, B, C
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 For Lead Free Parts, Device
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ELECTRICAL CHARACTERISTICS (T_a=25°C unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	
DC Current Gain	h _{FE}	I _C =10μA, V _{CE} =5V					
		A		90			
		B		150			
		C		270			
		I _C =2mA, V _{CE} =5V					
		BC546	110		450		
		BC547/548	110		800		
		A	110		220		
		B	200		450		
		C	420		800		
Collector Emitter Saturation Voltage	V _{CE (sat)}	I _C =10mA, I _B =0.5mA			0.25	V	
		I _C =100mA, I _B =5mA			0.60	V	
Base Emitter Saturation Voltage	V _{BE (sat)}	I _C =10mA, I _B =0.5mA		0.7		V	
		I _C =100mA, I _B =5mA		0.9		V	
Base Emitter On Voltage	V _{BE (on)}	I _C =2mA, V _{CE} =5V	0.55		0.70	V	
		I _C =10mA, V _{CE} =5V			0.77	V	

SMALL SIGNAL CHARACTERISTICS

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	
Transistors Frequency	f _T	I _C =10mA, V _{CE} =5V, f=100MHz		300		MHz	
Collector Output Capacitance	C _{cb0}	V _{CB} =10V, f=1MHz			4.5	pF	
Emitter Input Capacitance	C _{ib}	V _{EB} =0.5V, f=1MHz		9.0		pF	
Noise Figure	NF	I _C =0.2mA, V _{CE} =5V, R _S =1 kΩ, f=1KHz, B=200Hz			10	dB	
Small Signal Current Gain	h _{fe}	I _C =2mA, V _{CE} =5V, f=1KHz					
			A		220		
			B		330		
			C		600		
Input Impedance	h _{ie}	I _C =2mA, V _{CE} =5V, f=1KHz					
			A	1.6		4.5	kΩ
			B	3.2		8.5	kΩ
			C	6.0		15	kΩ
Voltage Feedback Ratio	h _{re}	I _C =2mA, V _{CE} =5V, f=1KHz					
			A		1.5		x10 ⁻⁴
			B		2.0		x10 ⁻⁴
			C		3.0		x10 ⁻⁴
Out Put Admittance	h _{oe}	I _C =2mA, V _{CE} =5V, f=1KHz					
			A			30	umhos
			B			60	umhos
			C			110	umhos

NPN SILICON PLANAR EPITAXIAL TRANSISTORS

BC546, A, B, C

BC547, A, B, C

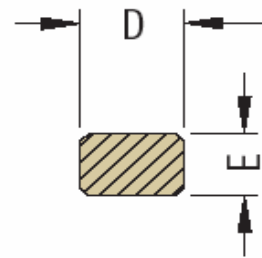
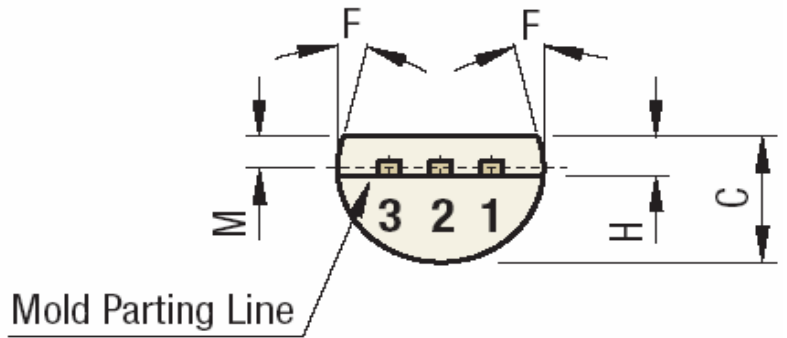
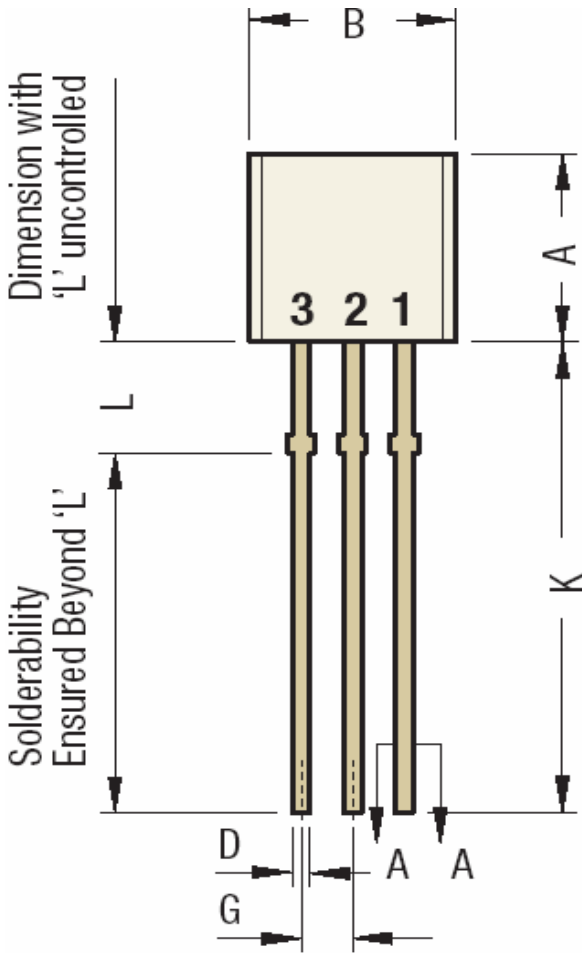
BC548, A, B, C

TO-92

Plastic Package

For Lead Free Parts, Device Part # will be Prefixed with "T"

TO-92 Leaded Plastic Package



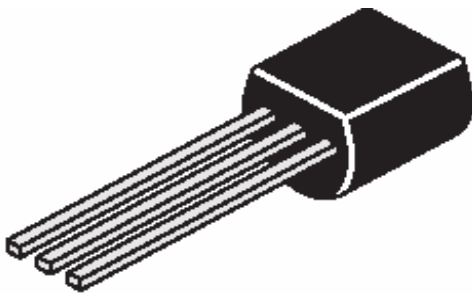
SEC AA

DIM	Min	Max
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.40	0.55
E	0.30	0.55
F	5°	

All Dimensions are in mm

DIM	Min	Max
G	1.14	1.40
H	1.20	1.80
K	12.5	
L	1.982	2.082
M	1.03	1.53

Pin 1 Emitter
Pin 2 Base
Pin 3 Collector



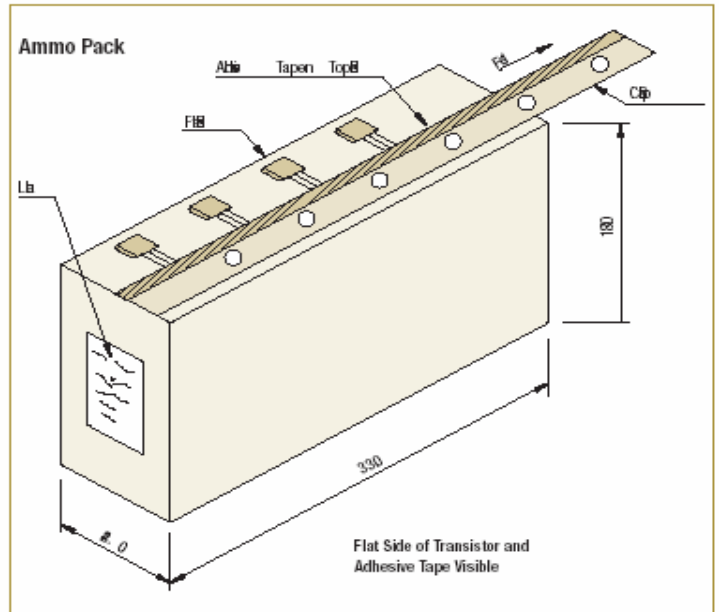
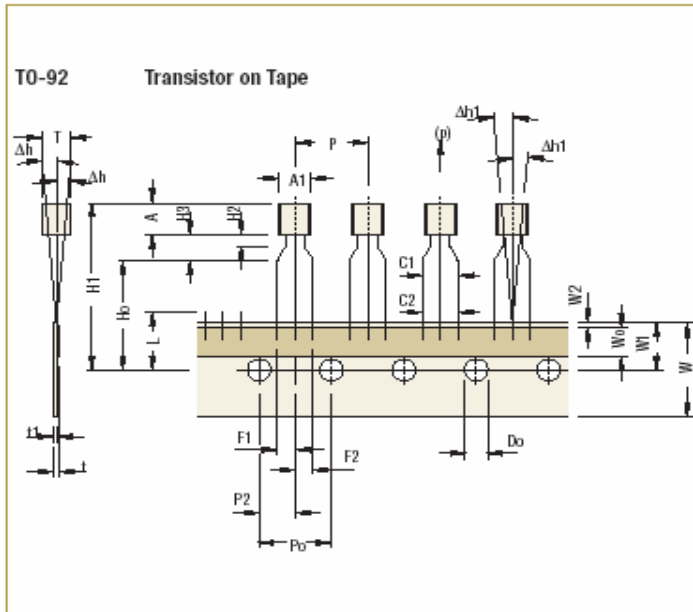
NPN SILICON PLANAR EPITAXIAL TRANSISTORS

BC546, A, B, C
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TO-92

Plastic Package

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TO-92 Tape and Ammo Packaging



All Dimensions are in mm

Tape Specifications

Item description	Symbol	TO-92			
		Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component ^{Cr}	P		12.7		±1.0
Feed hole pitch ^{§1}	Po		12.7		±0.3
Feed hole center to component centre ^{§2}	P2		6.35		±0.4
Comp. alignment, Side view ^{§3}	Dh		0	1.0	
Comp. alignment, Front view ^{§3}	Dh1		0	1.3	
Tape width ^{Cr}	W		18		±0.5
Hold down tape width ^{Cr}	W0		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of clipped leads	L			11.0	
Feed hole diameter ^{Cr}	Do		4		±0.2
Total tape thickness ^{§4}	t			1.2	
Lead-to-lead distance ^{Cr}	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelism ^{Cr}	C1-C2			0.22	
Pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.

§2 To be measured at bottom of clinch.

§3 At top of body.

§4 t1 = 0.3 – 0.6 mm

Cr Critical Dimension.

All Dimensions are in mm

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NPN SILICON PLANAR EPITAXIAL TRANSISTORS

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Plastic Package

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Packaging Information

T & A: Tape and Ammo Pack; T & R: Tape and Red; Bulk: Loose in Poly bags; Tube: Tube and Ammo Pack; k: 1.000

Package/Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Customer Notes

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s). CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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